In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-40. (Canceled)

41. (Currently Amended) A fabrication method for a semiconductor device, comprising the steps of:

providing a semiconductor substrate having a first metal layer;

forming an etch stop layer overlying the first metal layer and the semiconductor substrate, wherein the etch stop layer has a dielectric constant smaller than 3.5;

forming a dielectric layer overlying the etch stop layer, wherein the dielectric layer has a dielectric constant smaller than 3.0;

forming an opening which penetrates the dielectric layer and the etch stop layer and exposes the first metal layer; and

forming a second metal layer in the opening, in which the second metal layer is electrically connected to the first metal layer ~~The fabrication method for a semiconductor device of claim 29~~, wherein the etch stop layer is a SiOC layer, and forming the etch stop layer is by a plasma enhanced chemical vapor deposition having:

$SiH\text{-}(CH_3)_3$ with a flow rate of 50~300 sccm;

CO_2 with a flow rate of 300~500 sccm;

a process temperature of 350~400°C;

a process pressure of 8~10 Torr;

a high-frequency (HF) RF power of 300~500W; and

a low-frequency (LF) RF power of 60~200W.

42-47. (Canceled)

48. (Previously presented) A semiconductor device, comprising:

a semiconductor substrate;

a first metal layer formed overlying the semiconductor substrate;

a composite etch stop layer, comprising a first etch stop layer overlying a second etch stop layer, formed overlying the first metal layer and the semiconductor substrate;

a dielectric layer formed overlying the etch stop layer; and

a second metal layer penetrating the dielectric layer and the etch stop layer and electrically connected to the first metal layer;

wherein, the etch stop layer has a dielectric constant smaller than 3.5;

wherein, the dielectric layer has a dielectric constant smaller than 3.0;

wherein the dielectric layer has a tensile stress approximating to the compressive stress of the etch stop layer;

wherein the first etch stop layer is a SiCO film, and the second etch stop layer is a SiCO film;

wherein a first etching selectivity S_1 of the first etch stop layer to the dielectric layer, and a second etching selectivity S_2 of the second etch stop layer to the dielectric layer satisfy the formula: $S_1 \neq S_2$.

49. (Previously presented) The semiconductor device of claim 48, wherein the etch stop layer has a compressive stress of $0\sim1x10^9$ dynes/cm^2.

50. (Previously presented) The semiconductor device of claim 48, wherein the dielectric layer has a film hardness greater than 0.2GPa and an elastic modulus greater than 5GPa.

51. (Previously presented) The semiconductor device of claim 48, wherein S_1 and S_2 satisfy the formula: $0<S_1<S_2$.

52. (Previously presented) The semiconductor device of claim 48, wherein a first thickness T_1 of the first etch stop layer and a second thickness T_2 of the second etch stop layer satisfy the formula: $T_2 < (T_1+ T_2)/3$.